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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,741	11/04/2005	Ludwig Dittmar	2002 P 09188 US	9239

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EXAMINER	
DINH, THU HUONG T	
ART UNIT	**PAPER NUMBER**
2812	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/519,741	DITTMAR ET AL.	
	Examiner	Art Unit	
	Thu-Huong Dinh	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) *1-20 and 28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-27,29-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

WALTER LINDSAY JR
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/20/2006 has been entered.

Claims 1-20 are cancelled. Claims 21, 29, 30-31, 33-34 are amended. Currently, Claims 21- 27 and 29-35 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 21, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (U.S. 6720252 filed November 13, 2002) in view of Chiu (U.S. 2001/0051408 filed October 5, 1999).

Chen et al. background teach the following: 1) providing a first contact hole (108) in an insulating layer (106) (col. 2, lines 9-10); [[and]] filling the contact hole (108) with an ARC layer (110) that also overlies the insulating layer (106) (col.2, lines 13-14); depositing and patterning a photoresist layer (112) on said ARC layer

(110) (col. 2, lines 19-20); removing portions of the ARC layer (110) not covered by the photoresist layer (112) (col.2 lines 23-24); removing the ARC layer filling from the contact hole (108) (col. 2, lines 33-35); and filling the contact hole (108) with contact material (118) so that the contact material (118) is electrically connected to a line (col. 2, lines 35-37); (Claim 21); 2) ...providing said insulating layer (106) (col.2, lines 4-6); providing said hard mask patterned to form said contact hole(108); etching said contact hole (108) in said insulating layer (106) (col.2, lines. 8-13); re-patterning said hard mask subsequent to said step of covering the insulating layer with an ARC layer (110)to form said conductor trench connected to said contact hole (108) (col. 2, lines 23-24); etching said conductor trench (116) in said insulating layer (106) (col.2, lines 31-32); and filling said contact hole (108) and said conductor trench (116) with a conductive material (118) such that said conductive material in said conductor trench and said contact hole are electrically connected (col.2, lines 35-37 and Fig. 2C) (Claim 30).

Chen et al. lack the anticipation of explicitly teaching the following: 1)...wherein a hard mask that is used to pattern the contact hole is subsequently repatterned to define a conductor line trench which is connected thereto (Claim 21) 2)...re-patterning said hard mask subsequent to said step of covering the insulating layer with an ARC layer to form said conductor trench connected to said contact hole; (Claim 30).

Chiu teach Method for Providing Improved Step Coverage of Deep Trenches and Use Thereof. The invention relates to the deposition of films into

deep trenches, and more particularly to improving the step coverage of films deposited into deep trenches. As dimensions continue to be scaled down to the submicron level, the deep trench opening shrinks in size while the depth of the deep trench remains the same. In other word, the aspect ratio of deep trenches increases as semiconductor devices become more densely packed.

Chiu teach in Figure 4, a silicon oxide layer 22 is formed on the substrate 20 and silicon nitride layer 24 is formed on the silicon oxide layer 20 (col. 1, [0019]). The silicon oxide layer serves as a buffer for the stress induced by the silicon nitride layer 24 on the silicon substrate 20. The silicon oxide layer 22 and the silicon nitride layer 24 together constitute the so-called "hard mask" (col. 2, [0021]). Upon formation of the hard mask, steps for patterning the mask can be performed. The silicon nitride layer 24 and the silicon oxide layer 22 are removed at portions left exposed by a patterned photoresist by RIE using a plasma formed from, for example, CHF_3/CF_4 source gas. An opening 26 through the hard mask is formed to expose portions of surface areas on the silicon substrate 20 (col.2, [0022]). The patterned hard mask then used to form deep trenches 28 as holes etched into the silicon substrate 20 by RIE using a plasma formed from CF_4 source gas. The resulting trench structure is shown in Fig. 5 (col. 2, [0023]).

It would be obvious to one of ordinary skill in the art, at the time of invention was made, to modify the structure shown in Chen et al. with Chiu's teaching of providing improved step coverage of deep trenches with the

motivation of the deposition of films produces good step coverage into a deep trench having high aspect ratio.

4. Claims 24 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (U.S. 6720252 filed November 13, 2002) in view of Chiu (U.S. 2001/0051408 filed October 5, 1999) as applied to claims 21 and 30 above, and further in view of Carey (U.S. 5,173,442 dated December 22, 1992).

Chen et al. and Chiu teaches the structure as claimed and as described in the preceding paragraphs; however, Chen et al. and Chiu lack anticipation only in not explicitly the teaching of: 1) ...wherein said dry etching process comprises using at least one of the group SF_6, HBr and He/O_2 (Claims 24, 32).

Carey teaches the Methods of Forming Channels and Vias in Insulating Layers. The channels extending partially through and vias extending completely through an insulation layer in an electrical interconnect such as a substrate can be formed in a relatively few steps with low cost etching and patterning techniques. In Figure 1a, a thin blanket layer of metal is sputtered over the insulation layer as polyimide layer (14) to form hard mask (16), which after conventional patterning has openings to expose via regions (20) and channel region (22) (column 3, lines 44-50). As plasma etch (24) is applied hard mask (16) etches slowly (column 3, lines 59-60) and plasma etch (24) can comprise 90% O2 and 10% SF6 (column 4, lines 3). While dry etching with plasma etches is the preferred method of etching, other etching methods is suitable for selectively removing material from the insulating layer (column 4, lines 42-45).

It would be obvious to one of ordinary skill in the art, at the time of invention was made, to modify the structure shown in Wang et al. with Carey's teaching of forming vias in an insulation layer with the motivation of reducing cost in etching and patterning techniques.

5. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (U.S. 6720252 filed November 13, 2002) in view of Chiu (U.S. 2001/0051408 filed October 5, 1999) as applied to claims 21 and 30 above, and further in view of Matsuoka et al. (U.S. 613049 filed October 10, 2000).
Chen et al. and Chiu teaches the structure as claimed and as described in the preceding paragraphs; however, Chen et al. and Chiu lack anticipation only in not explicitly the teaching of: 1) ... further comprising the step of depositing a liner on a surface of said contact hole and conductor trench prior to said step of filling (Claim 33).

Matsuoka et al. teaches Semiconductor Memory Device and a Method for Fabricating the Same. To achieve a memory cell on a smaller scale, the three-dimensional structure of a capacitor has been adopted in generations after the fourth generation in order to secure a larger capacitance in a smaller area. In the photolithography step, the depth of focus becomes smaller as the resolution is increased in order to achieve a finer pattern. Thus, the linewidth being a key element in a technology of miniaturization to be employed in the next generation of memory devices. In Figure 13, a silicon oxide film (901) is formed as an interlayer insulating film in such manner that the silicon oxide film (901) may cover the bitlines (601A) and interconnect metallization (610B). Contact hole for

the storage nodes are further formed in the silicon oxide film (901) and TiN plug (502) (Figure 17) is formed in a contact hole for a storage node (column 7, lines 17-26). In Figure 3, a shallow trench isolation region (2) is formed on a main surface of the substrate (1) (column 8, lines 54-56) and depositing a silicon oxide film with a thickness of about 0.4 microns by means of a known CVD method; selective polishing off the oxide film formed on a region other than the trenches (column 8, lines 59-63). In Figure 17, TiN (502) was deposited on the surface with openings of the contact holes (1001) by means of CVD (column 10, lines 41-43).

It would be obvious to one of ordinary skill in the art, at the time of invention was made, to modify the structure shown in Wang et al. with Matsuoka et al. teaching of forming a dynamic random access memory device which is suitable for a higher integration complexity.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

7. Claims 22-23, 25-27, 29, 31 and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Prior Art, Gruening-Von Schwerin et al. U.S.2004/0206722 filed April 18, 2002).

8. The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Prior Art, Gruening-Von Schwerin et al. teaches a semiconductor substrate (column 2 [0024]) providing a first contact hole (K1) in an insulating layer (column 3 [0026]); and filling the contact hole (K1) with contact material (60) (column 5 [0060]) so that the contact material is electrically connected to a line (column 4 and column 5 [0056]); wherein a hard mask (M1) that is used to pattern the contact hole (column 5 [0057]) is subsequently re-patterned (column 5 [0058]) to define a conductor line trench (70) which is connected thereto (column 5 [0062]). Preferably, the hard mask (M1) is made from polycrystalline silicon (column 4 [0055]) (Claim 22, 29) and further comprising patterning said hard mask by means of a dry etching process (column 5 [0059]) (Claims 23,31). Prior Art, Gruening-Von Schwerin et al. teaches depositing a liner on a surface of said contact hole (K1) and line prior to said step of filling holes with Tungsten (column 5 [0062]) (Claims 25, 27and 34) and the liner is selected from the group consisting of Ti and TiN (column 5 [0062]) (Claims 26, 35).

Allowable Subject Matter

9. The indicated allowability of claim 30 is withdrawn in view of the newly discovered reference(s) to Chiu (U.S.2001/0051408 Pub. Date Dec. 13, 2001). Rejections based on the newly cited reference(s) above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thu-Huong Dinh whose telephone number is 571 272-9014. The examiner can normally be reached on Monday through Friday (8:30AM-5:00PM Eastern).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

WALTER LINDSAY JR.
PRIMARY EXAMINER